
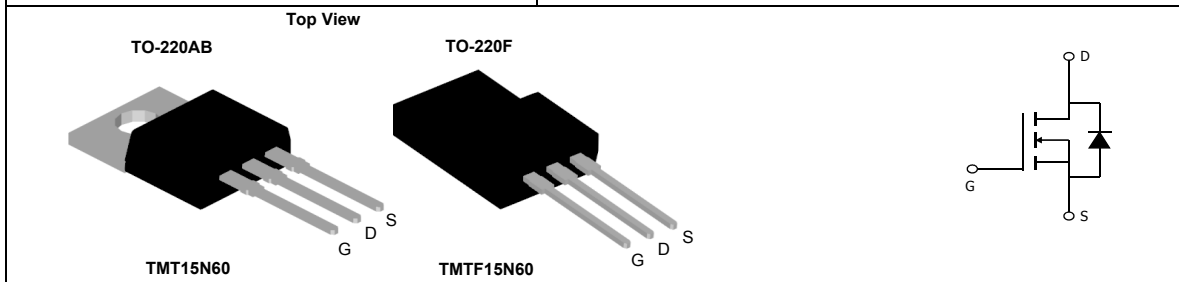


TMT15N60 / TMTF15N60 N-CHANNEL POWER MOSFET

<p>General Description</p> <p>The TMT15N60 & TMTF15N60 have been fabricated using the advanced αMOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.</p>	<p>Product Summary</p> <table border="0"> <tr> <td>V_{DS}</td> <td>600V</td> </tr> <tr> <td>I_D</td> <td>15A</td> </tr> <tr> <td>$R_{DS(ON),max}$</td> <td>0.29Ω</td> </tr> </table> <p>100% UIS Tested 100% R_g Tested</p> 	V_{DS}	600V	I_D	15A	$R_{DS(ON),max}$	0.29 Ω
V_{DS}	600V						
I_D	15A						
$R_{DS(ON),max}$	0.29 Ω						



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted				
Parameter	Symbol	TMT15N60	TMTF15N60	Units
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current	I_D	$T_c=25^\circ\text{C}$	15	15*
		$T_c=100^\circ\text{C}$	10	10*
Pulsed Drain Current ^C	I_{DM}	63		A
Avalanche Current ^C	I_{AR}	2.4		A
Repetitive avalanche energy ^C	E_{AR}	86		mJ
Single pulsed avalanche energy ^G	E_{AS}	173		mJ
Power Dissipation ^B	P_D	$T_c=25^\circ\text{C}$	208	70
		Derate above 25°C	1.67	0.22
MOSFET dv/dt ruggedness	dv/dt	100		V/ns
Peak diode recovery dv/dt ^H	dv/dt	20		V/ns
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds ^J	T_L	300		$^\circ\text{C}$
Thermal Characteristics				
Parameter	Symbol	TMT15N60	TMTF15N60	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	$^\circ\text{C/W}$
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	—	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.6	4.5	$^\circ\text{C/W}$

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V	-	-	1	μA
		V _{DS} =480V, T _J =150°C	-	10	-	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.5	3.2	3.8	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7.5A, T _J =25°C	-	0.254	0.29	Ω
		V _{GS} =10V, I _D =7.5A, T _J =150°C	-	0.68	0.78	Ω
V _{SD}	Diode Forward Voltage	I _S =7.5A, V _{GS} =0V, T _J =25°C	-	0.83	-	V
I _S	Maximum Body-Diode Continuous Current		-	-	15	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C		-	-	63	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	717	-	pF
C _{OSS}	Output Capacitance		-	58	-	pF
C _{O(er)}	Effective output capacitance, energy related ^H	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz	-	41.2	-	pF
C _{O(tr)}	Effective output capacitance, time related ^I		-	125.2	-	pF
C _{rSS}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	1.3	-	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	13.4	-	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =7.5A	-	15.6	-	nC
Q _{gs}	Gate Source Charge		-	3.5	-	nC
Q _{gd}	Gate Drain Charge		-	6.0	-	nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =400V, I _D =7.5A, R _G =25Ω	-	24.5	-	ns
t _r	Turn-On Rise Time		-	22	-	ns
t _{D(off)}	Turn-Off Delay Time		-	84	-	ns
t _f	Turn-Off Fall Time		-	24	-	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =7.5A, di/dt=100A/μs, V _{DS} =400V	-	282	-	ns
I _{rm}	Peak Reverse Recovery Current	I _F =7.5A, di/dt=100A/μs, V _{DS} =400V	-	26	-	A
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =7.5A, di/dt=100A/μs, V _{DS} =400V	-	4.5	-	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=2.4A, V_{DD}=150V, Starting T_J=25°C

H. C_{O(er)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

I. C_{O(tr)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. Wavesoldering only allowed at leads.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

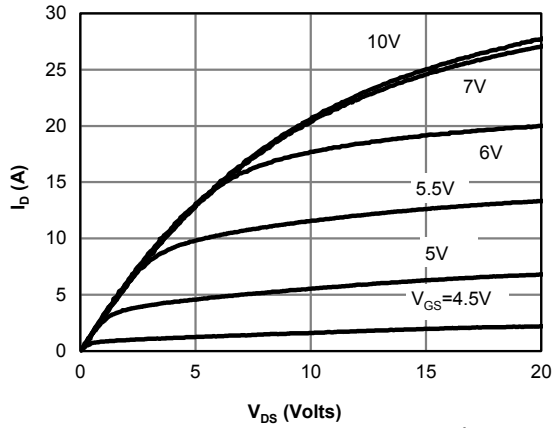


Figure 1: On-Region Characteristics@25° C

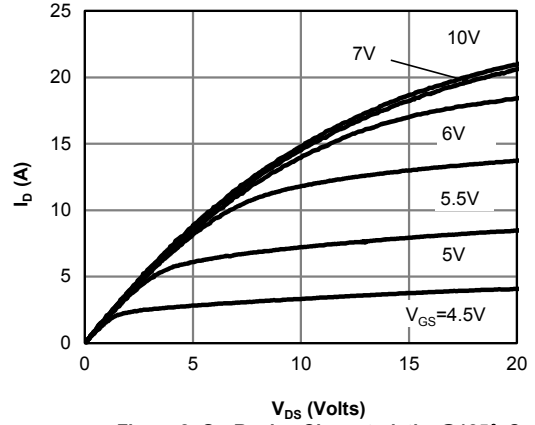


Figure 2: On-Region Characteristics@125° C

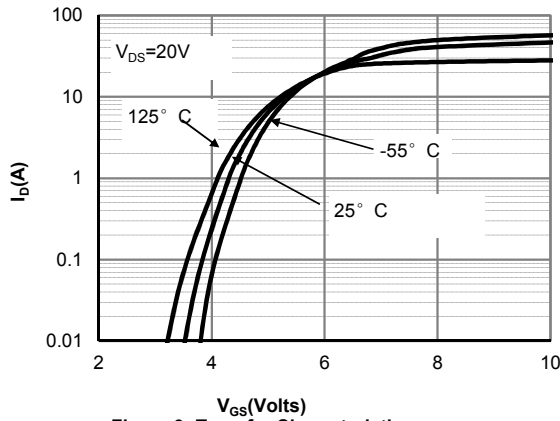


Figure 3: Transfer Characteristics

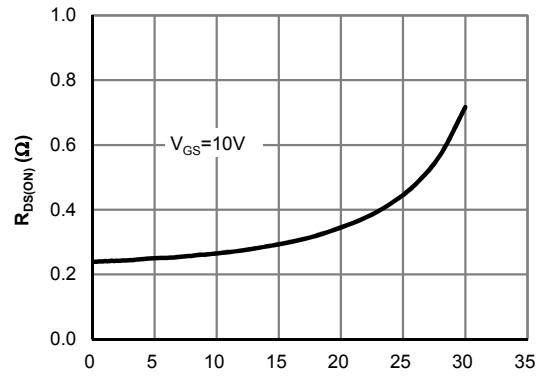


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

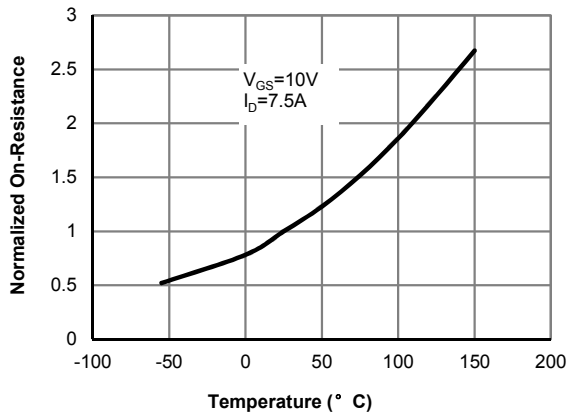


Figure 5: On-Resistance vs. Junction Temperature

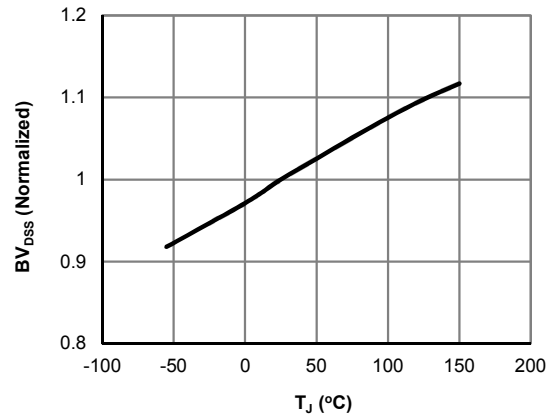


Figure 6: Break Down vs. Junction Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

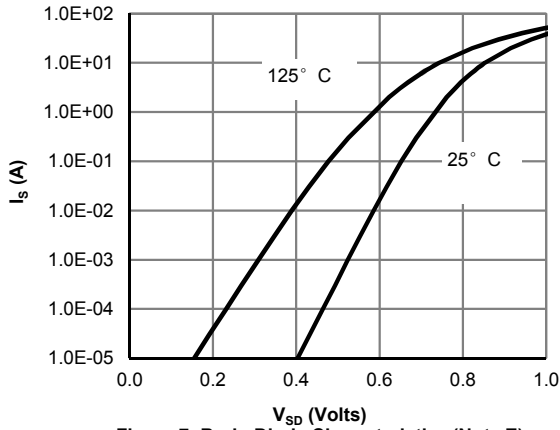


Figure 7: Body-Diode Characteristics (Note E)

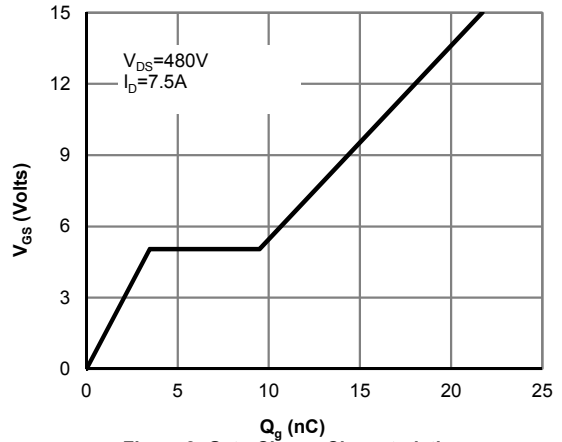


Figure 8: Gate-Charge Characteristics

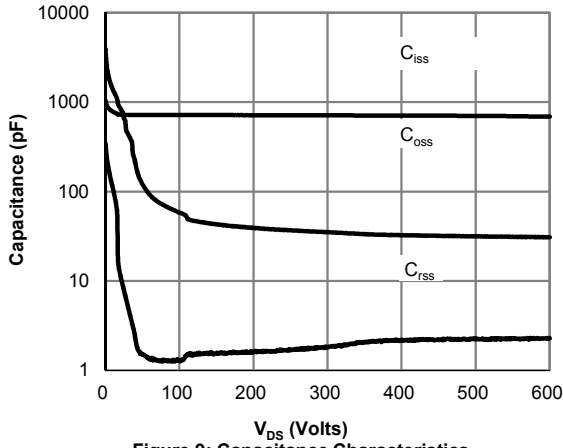


Figure 9: Capacitance Characteristics

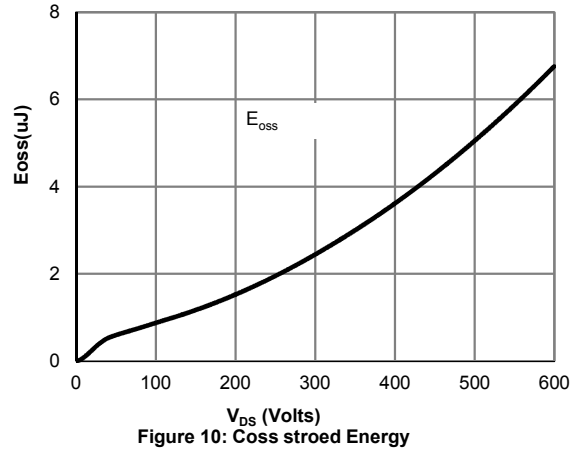


Figure 10: Coss stored Energy

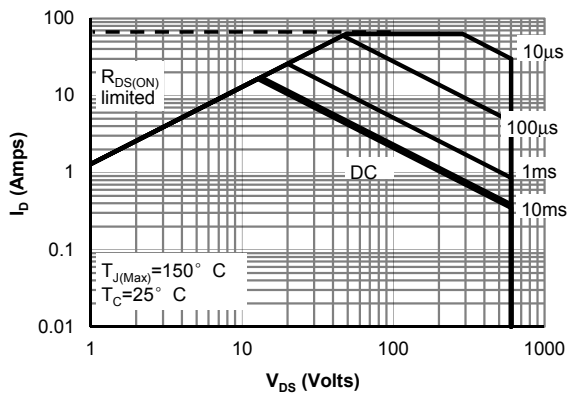


Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)15S60L (Note F)

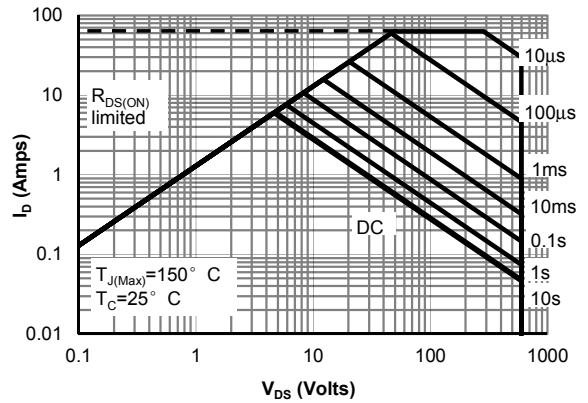


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF15S60L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

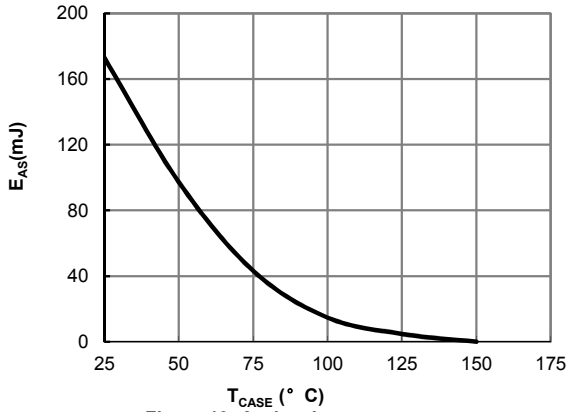


Figure 13: Avalanche energy

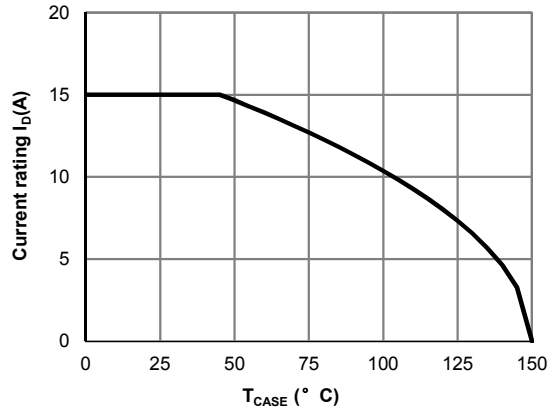


Figure 14: Current De-rating (Note B)

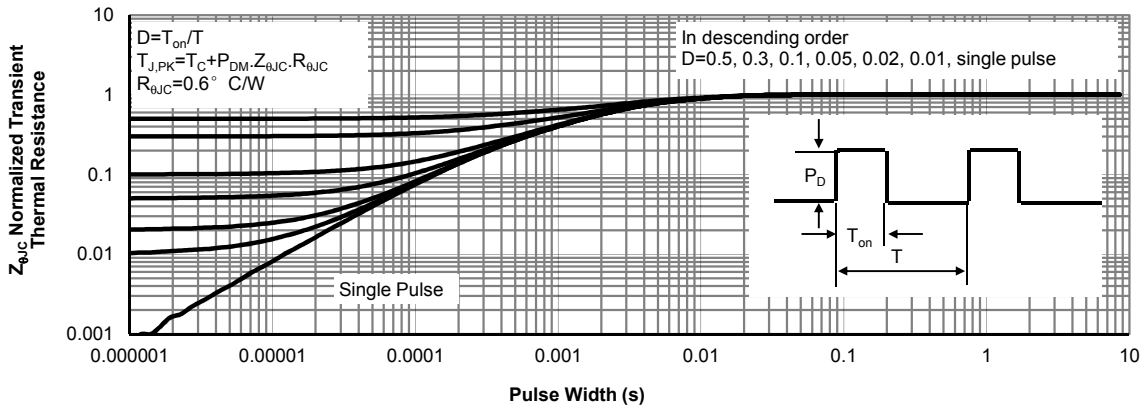


Figure 15: Normalized Maximum Transient Thermal Impedance for AOT(B)15S60 (Note F)

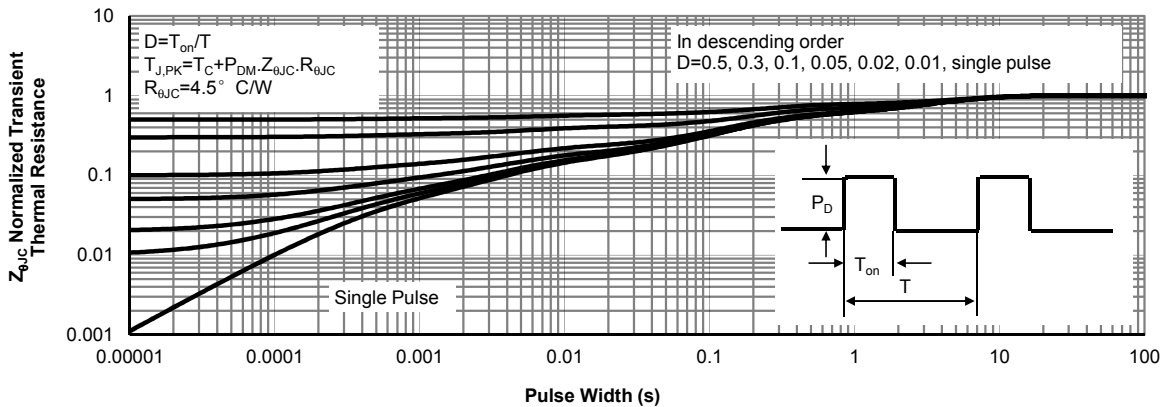
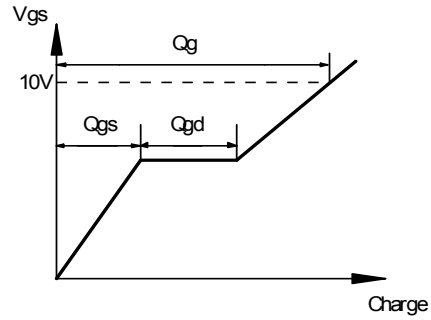
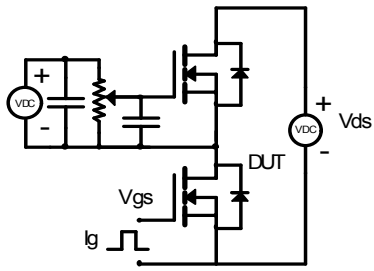
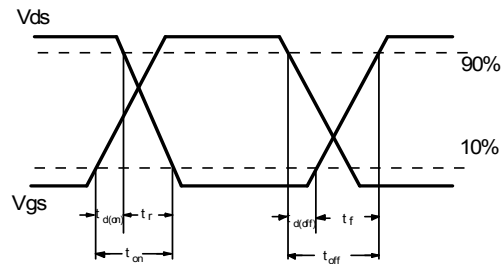
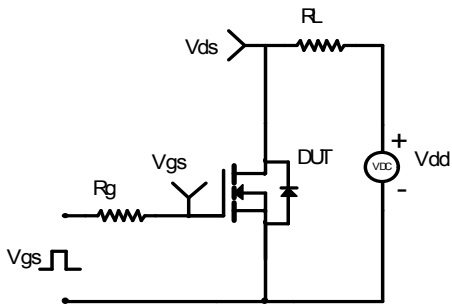


Figure 16: Normalized Maximum Transient Thermal Impedance for AOTF15S60L (Note F)

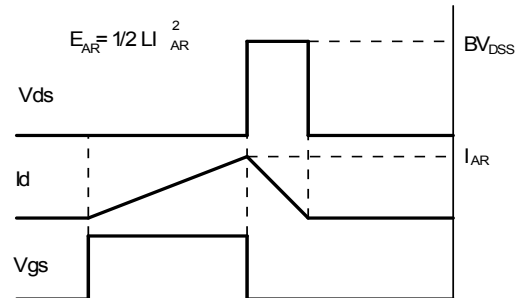
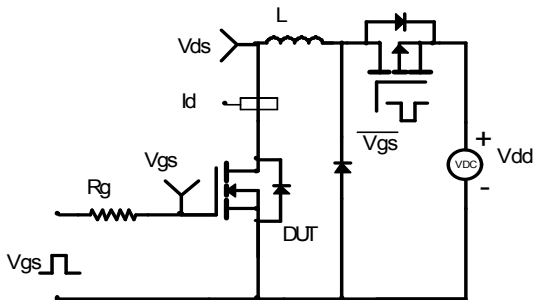
Gate Charge Test Circuit & Waveform



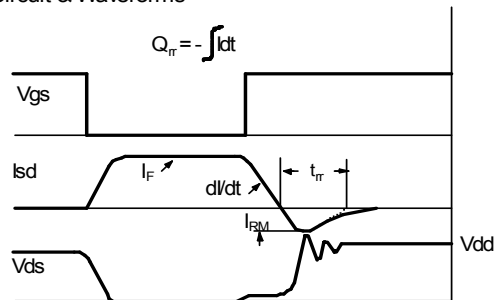
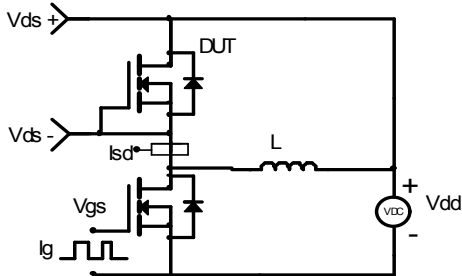
Resistive Switching Test Circuit & Waveforms



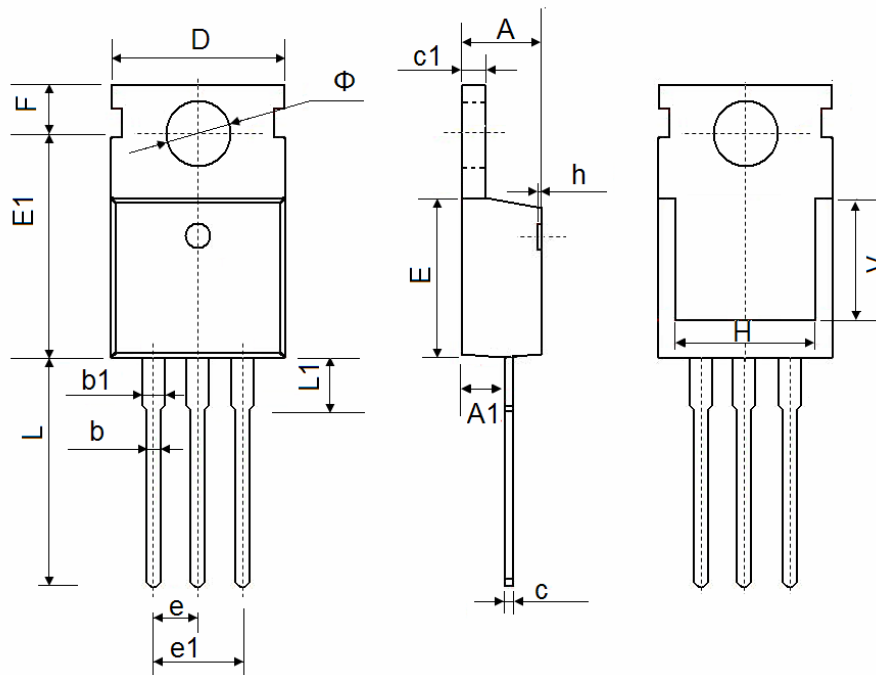
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

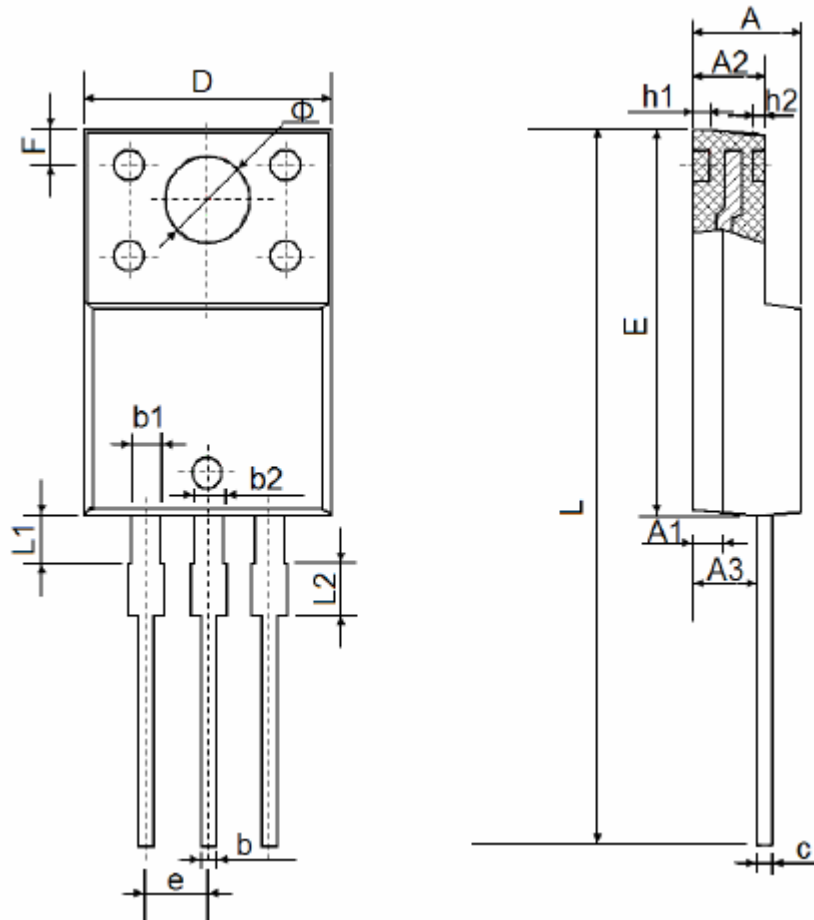


TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

TO-220F Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300REF		0.051REF	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540TYP.		0.100TYP	
F	2.700REF		0.106REF	
Φ	3.500REF		0.138REF	
h1	0.800REF		0.031REF	
h2	0.500REF		0.020REF	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083