
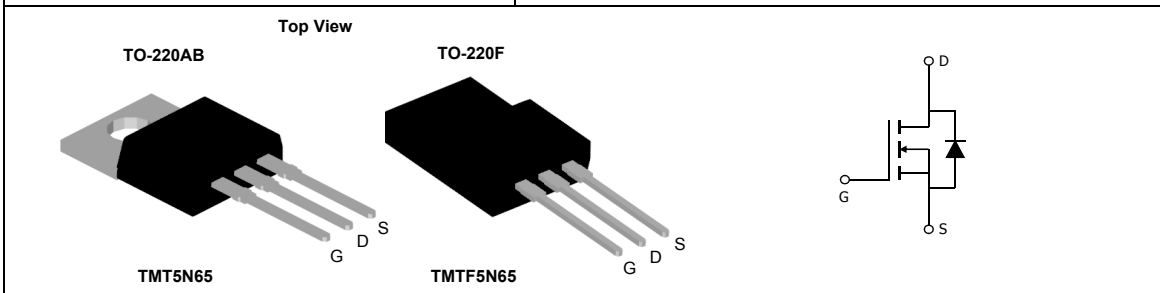


TMT5N65 / TMTF5N65 N-CHANNEL POWER MOSFET

<p>General Description</p> <p>The TMT5N65 & TMTF5N65 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.</p>	<p>Product Summary</p> <table style="width: 100%; border: none;"> <tr> <td style="width: 70%;">V_{DS}</td> <td style="text-align: right;">650V</td> </tr> <tr> <td>I_D (at $V_{GS}=10V$)</td> <td style="text-align: right;">5A</td> </tr> <tr> <td>$R_{DS(on)}$ (at $V_{GS}=10V$)</td> <td style="text-align: right;">< 3.0Ω</td> </tr> </table> <p>100% UIS Tested 100% R_{θ} Tested</p> <div style="text-align: right;">  </div>	V_{DS}	650V	I_D (at $V_{GS}=10V$)	5A	$R_{DS(on)}$ (at $V_{GS}=10V$)	< 3.0 Ω
V_{DS}	650V						
I_D (at $V_{GS}=10V$)	5A						
$R_{DS(on)}$ (at $V_{GS}=10V$)	< 3.0 Ω						



Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted				
Parameter	Symbol	TMT5N65	TMTF5N65	Units
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current	I_D	$T_C=25^{\circ}C$	5	A
		$T_C=100^{\circ}C$	3.15	
Pulsed Drain Current ^C	I_{DM}	20		A
Avalanche Current ^C	I_{AR}	2.5		A
Repetitive avalanche energy ^C	E_{AR}	94		mJ
Single pulsed avalanche energy ^G	E_{AS}	188		mJ
MOSFET dv/dt ruggedness	dv/dt	50		V/ns
Peak diode recovery dv/dt		5		
Power Dissipation ^B	P_D	$T_C=25^{\circ}C$	120	W
		Derate above 25 $^{\circ}C$	0.83	W/ $^{\circ}C$
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^{\circ}C$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300		$^{\circ}C$
Thermal Characteristics				
Parameter	Symbol	TMT5N65	TMTF5N65	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	$^{\circ}C/W$
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	$^{\circ}C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	3.6	$^{\circ}C/W$

^A Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	650			V
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.69		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =650V, V _{GS} =0V V _{DS} =480V, T _J =125°C			1 10	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3	4	4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2A		2.3	3.0	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =2A		7.4		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				5	A
I _{SM}	Maximum Body-Diode Pulsed Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	400	511	615	pF
C _{oss}	Output Capacitance		40	51	65	pF
C _{rss}	Reverse Transfer Capacitance		3.5	4.4	5.3	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.3	4.2	6.3	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =4A		15	18	nC
Q _{gs}	Gate Source Charge		3	3.6	nC	
Q _{gd}	Gate Drain Charge		7.6	9.1	nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =300V, I _D =4A, R _G =25Ω		20.2	30	ns
t _r	Turn-On Rise Time		28.7	42	ns	
t _{D(off)}	Turn-Off DelayTime		36	51	ns	
t _f	Turn-Off Fall Time		27	40	ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =4A, dI/dt=100A/μs, V _{DS} =100V		212	254	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =4A, dI/dt=100A/μs, V _{DS} =100V		1.6	1.9	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C, Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=2.5A, V_{DD}=150V, R_G=25Ω, Starting T_J=25° C

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

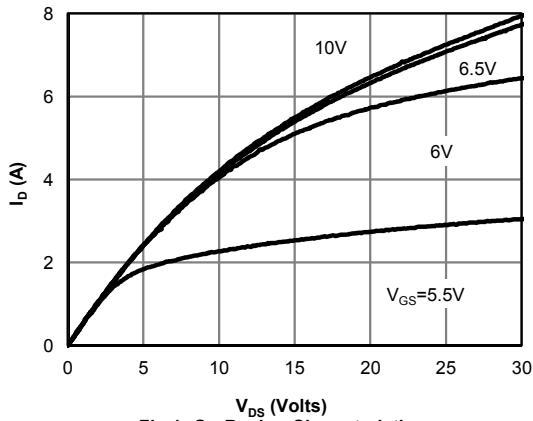


Fig 1: On-Region Characteristics

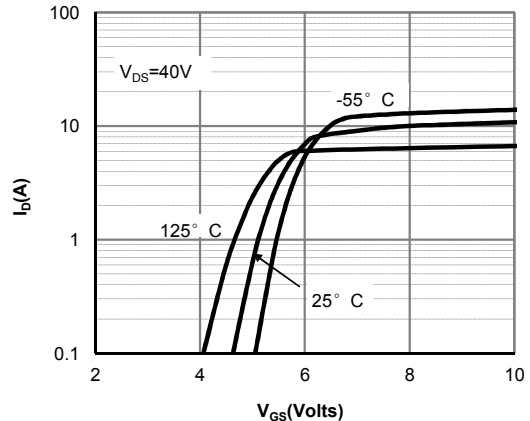


Figure 2: Transfer Characteristics

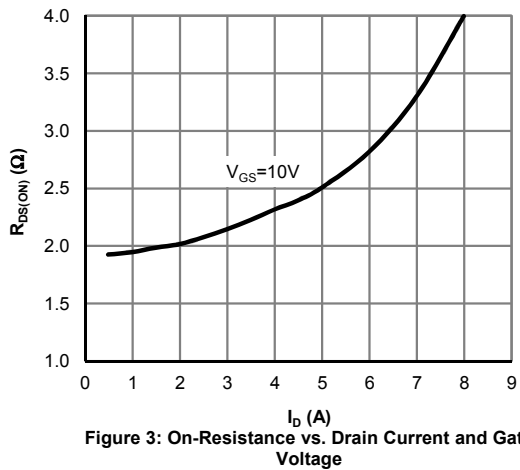


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

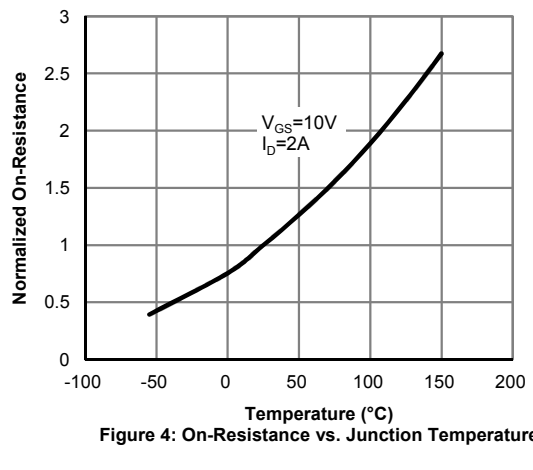


Figure 4: On-Resistance vs. Junction Temperature

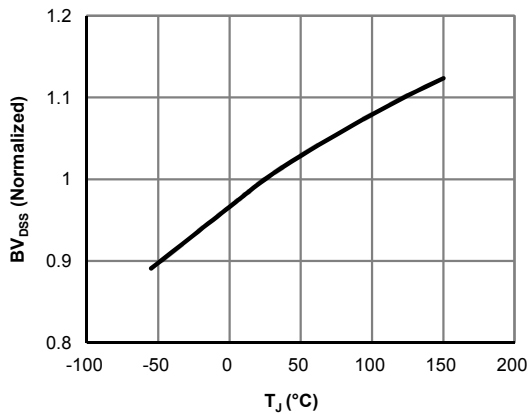


Figure 5: Break Down vs. Junction Temperature

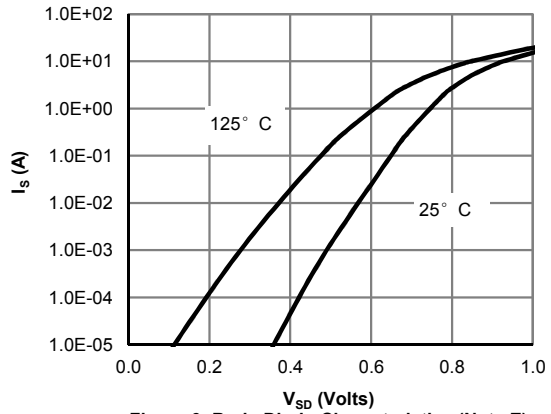


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

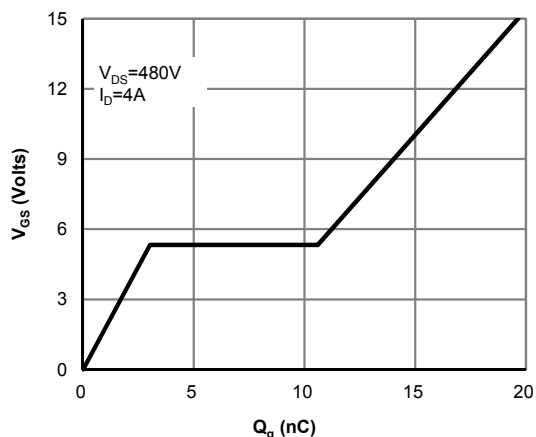


Figure 7: Gate-Charge Characteristics

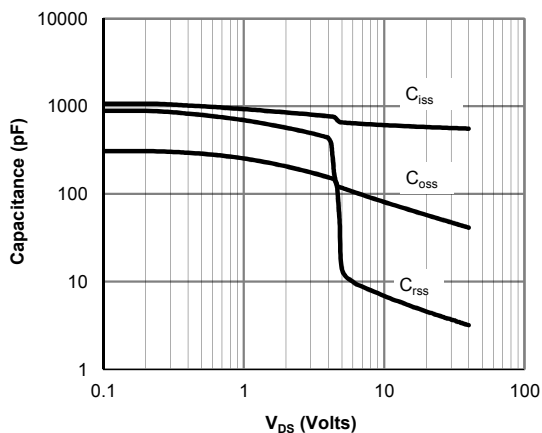


Figure 8: Capacitance Characteristics

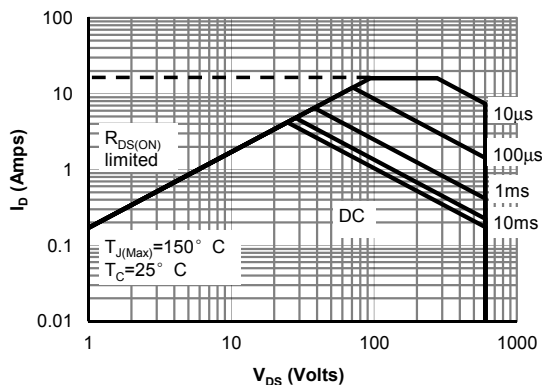


Figure 9: Maximum Forward Biased Safe Operating Area for AOT4N60 (Note F)

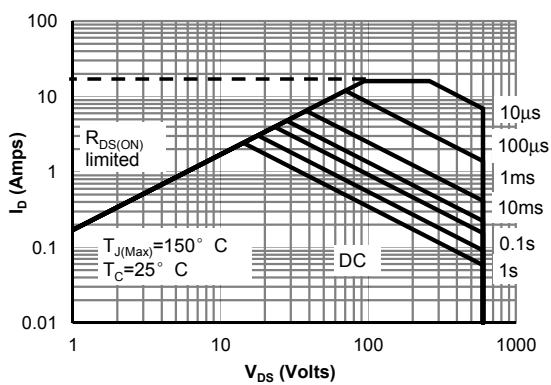


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF4N60 (Note F)

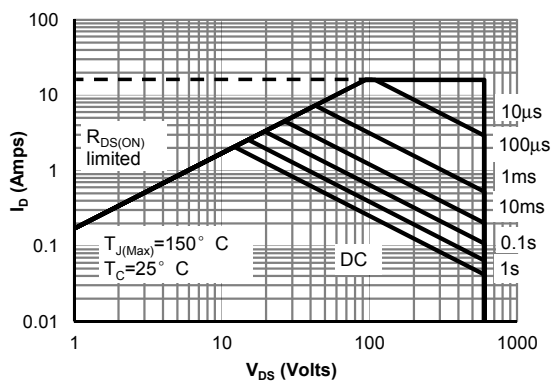


Figure 11: Maximum Forward Biased Safe Operating Area for AOTF4N60L (Note F)

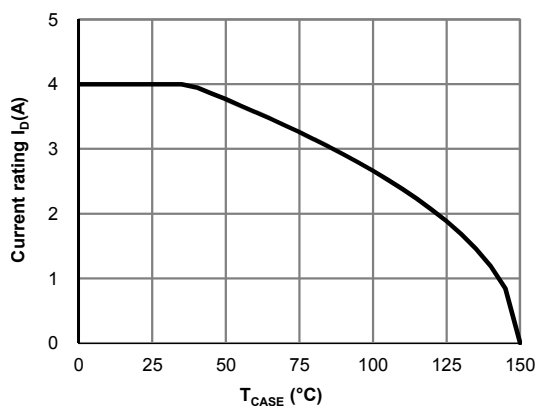


Figure 12: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

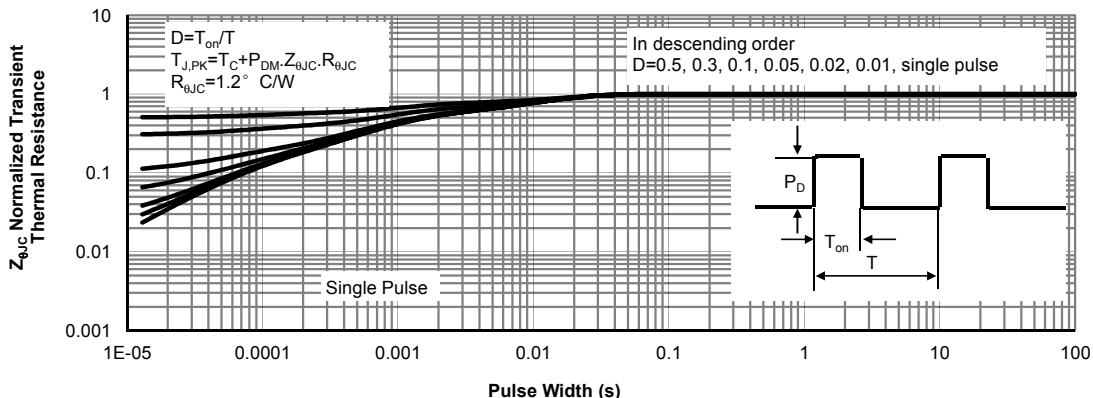


Figure 13: Normalized Maximum Transient Thermal Impedance for AOT4N60 (Note F)

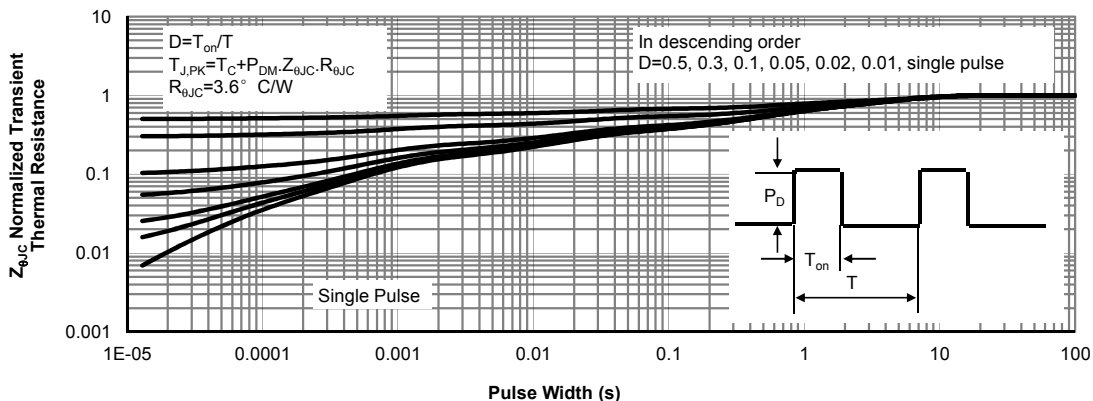


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF4N60 (Note F)

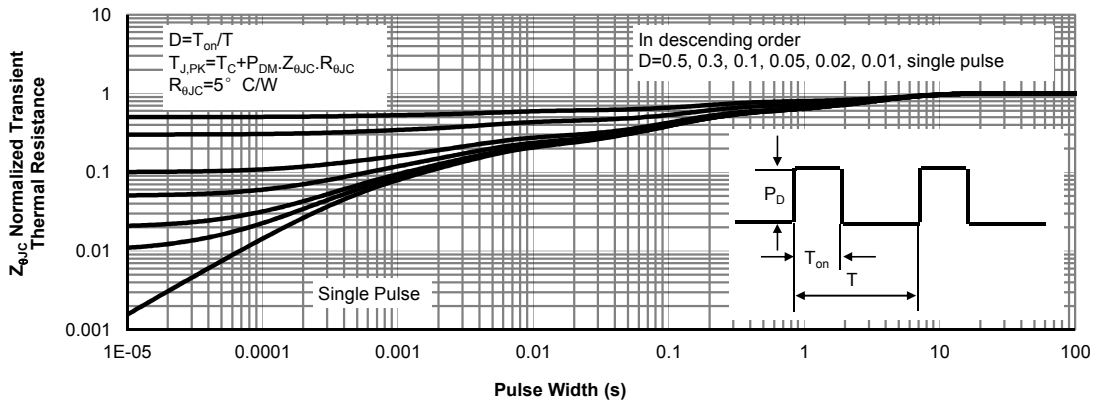
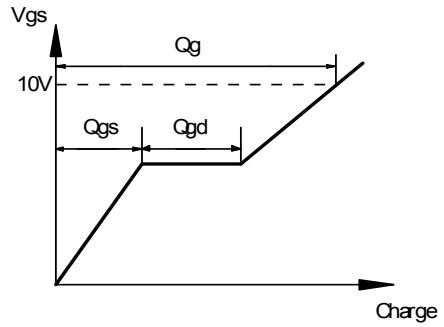
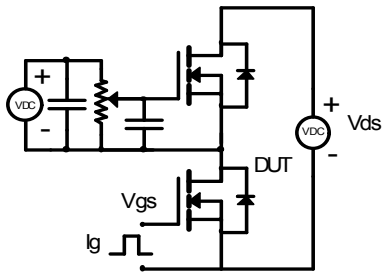
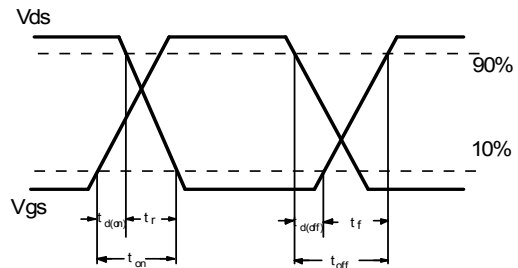
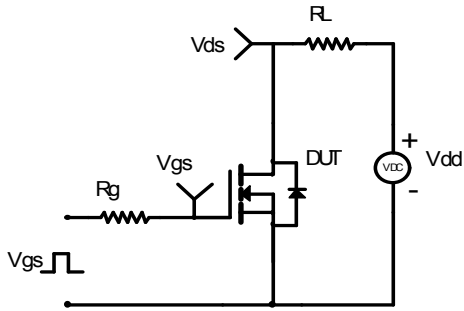


Figure 15: Normalized Maximum Transient Thermal Impedance for AOTF4N60L (Note F)

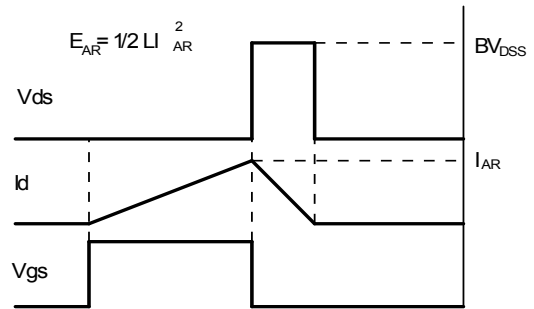
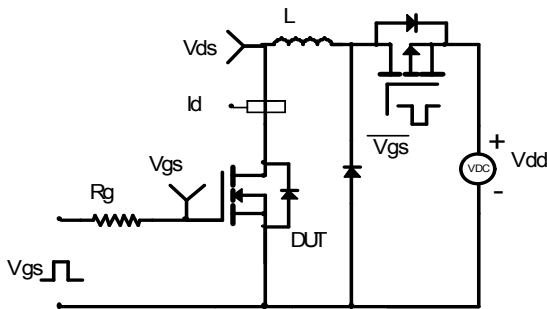
Gate Charge Test Circuit & Waveform



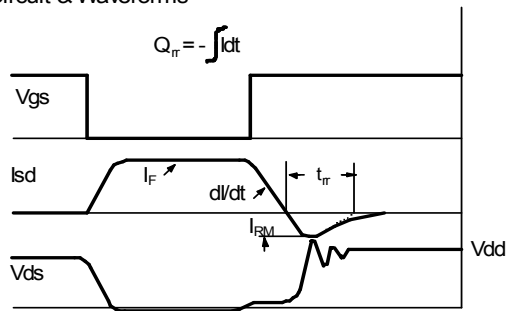
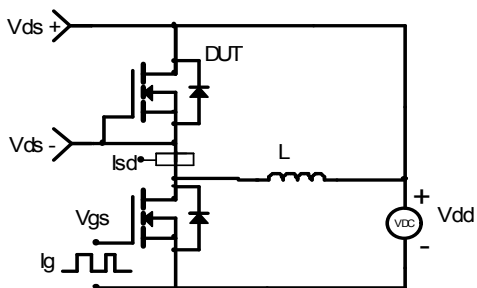
Resistive Switching Test Circuit & Waveforms



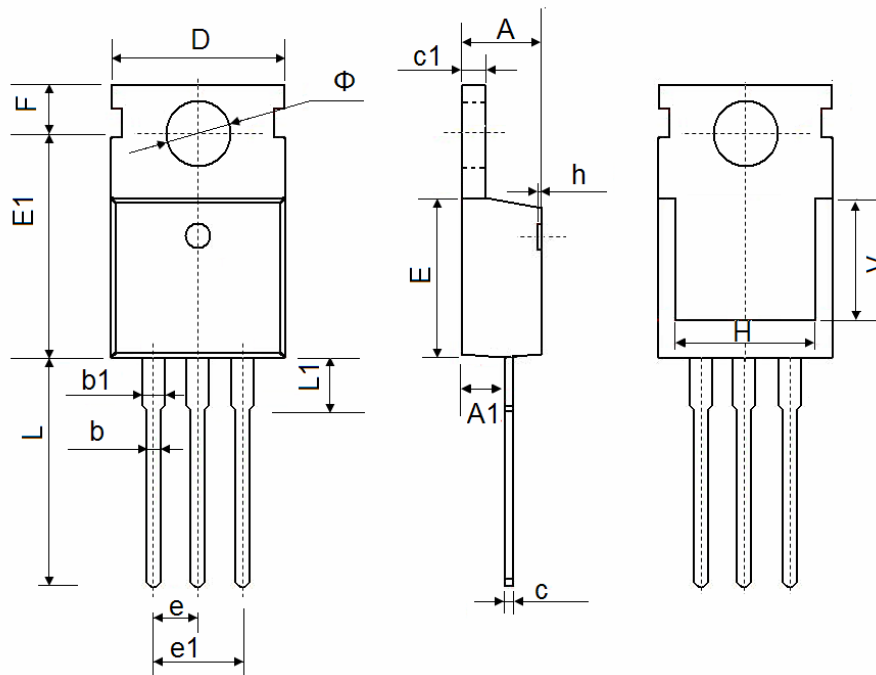
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

TO-220F Package Information