



## TMB80N08 N-CHANNEL POWER MOSFET

### General Description

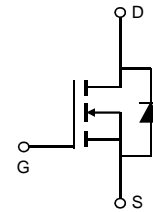
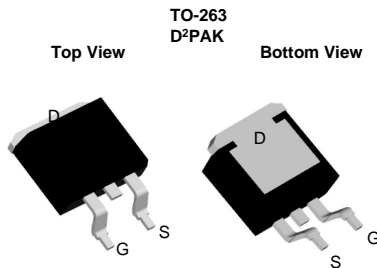
The TMB80N08 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

### Product Summary

$V_{DS}$	80V
$I_D$ (at $V_{GS}=10V$ )	80A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 9mΩ

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current-Continuous	$I_D$	80	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	55	A
Pulsed Drain Current	$I_{DM}$	280	A
Maximum Power Dissipation	$P_D$	200	W
Derating factor		1.33	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	800	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.75	$^{\circ}\text{C}/\text{W}$
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

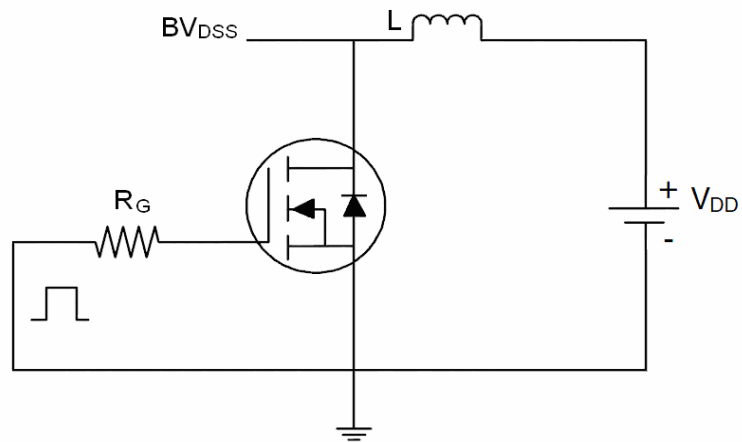
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	7	9	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=25V, I_D=40A$	80	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4900	-	PF
Output Capacitance	$C_{OSS}$		-	410	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	315	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega,$ $R_G=2.5\Omega, V_{GS}=10V$	-	20	-	nS
Turn-on Rise Time	$t_r$		-	19	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	$t_f$		-	30	-	nS
Total Gate Charge	$Q_g$	$I_D=30A, V_{DD}=30V, V_{GS}=10V$	-	125	-	nC
Gate-Source Charge	$Q_{gs}$		-	24	-	nC
Gate-Drain Charge	$Q_{gd}$		-	49	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	80	A
Reverse Recovery Time	$t_{rr}$	$T_j=25^{\circ}\text{C}, I_F=75A,$ $di/dt=100A/\mu S$ <sup>(Note 3)</sup>	-	37		nS
Reverse Recovery Charge	$Q_{rr}$		-	58		nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

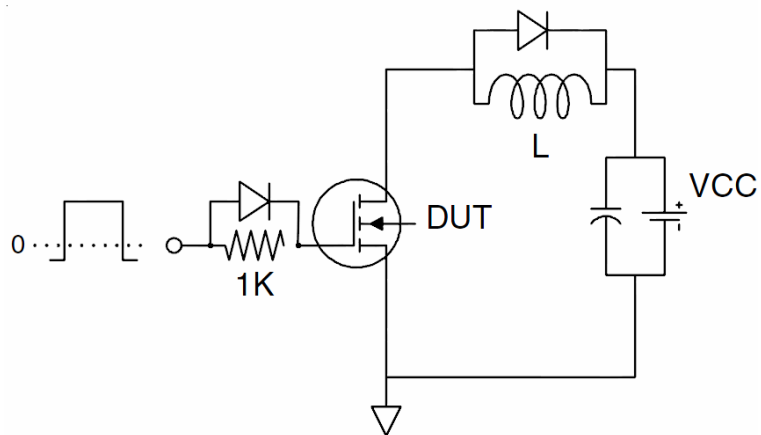
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_j=25^{\circ}\text{C}, V_{DB}=40V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

## Test circuit

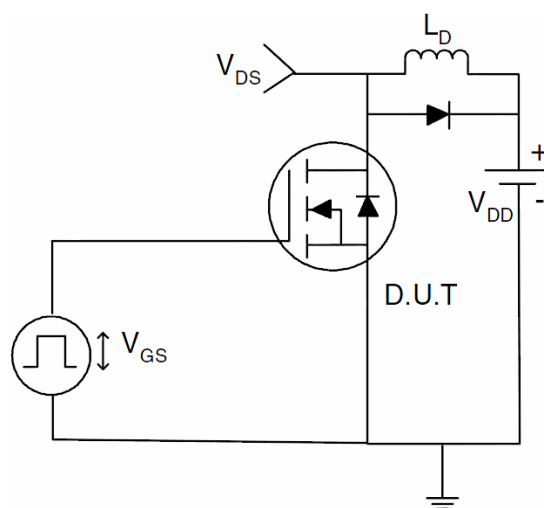
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

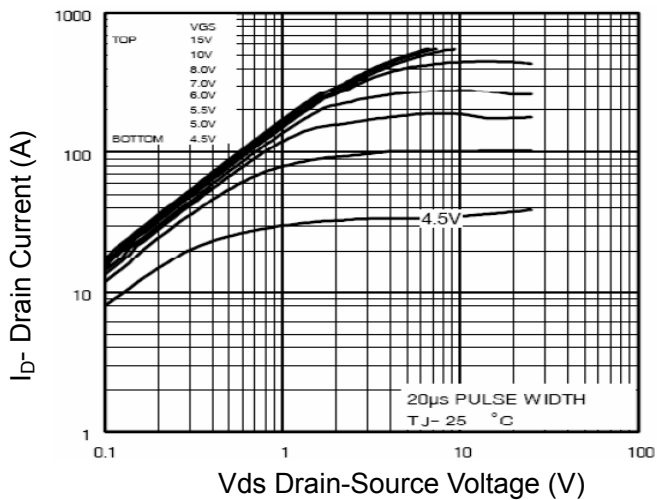


Figure 1 Output Characteristics

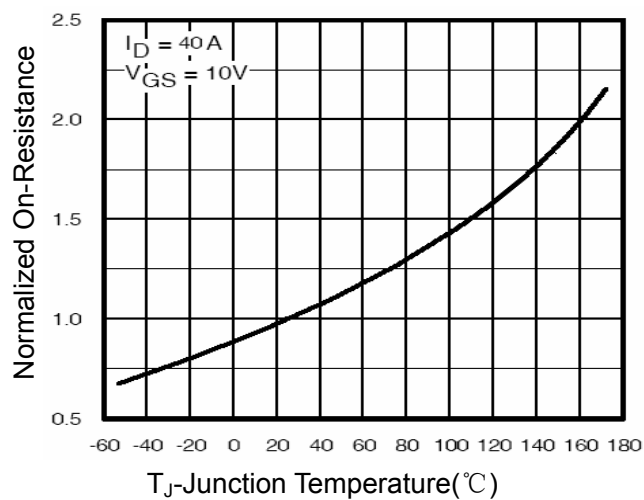


Figure 4  $R_{dson}$ -Junction Temperature

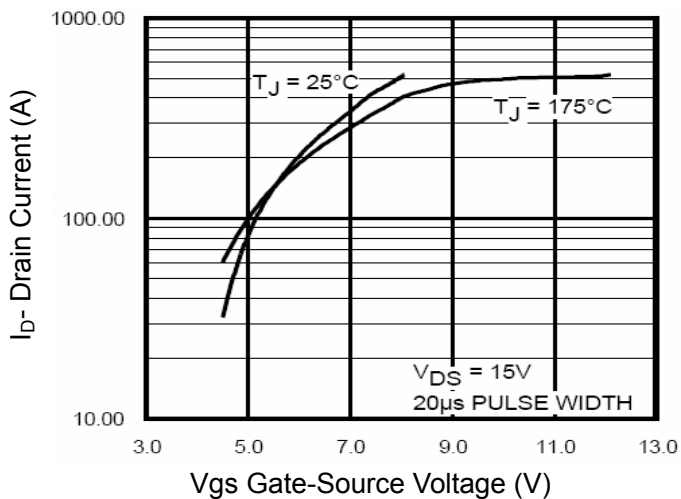


Figure 2 Transfer Characteristics

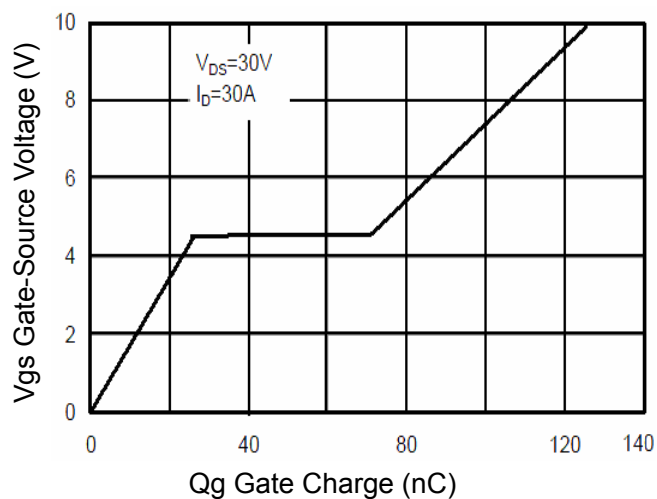


Figure 5 Gate Charge

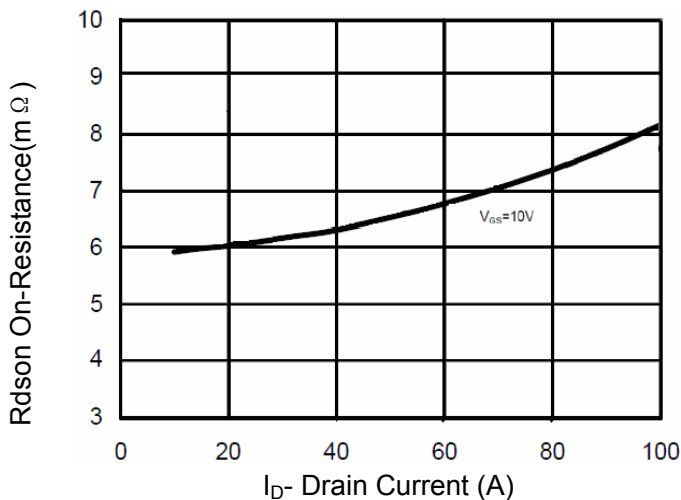


Figure 3  $R_{dson}$ - Drain Current

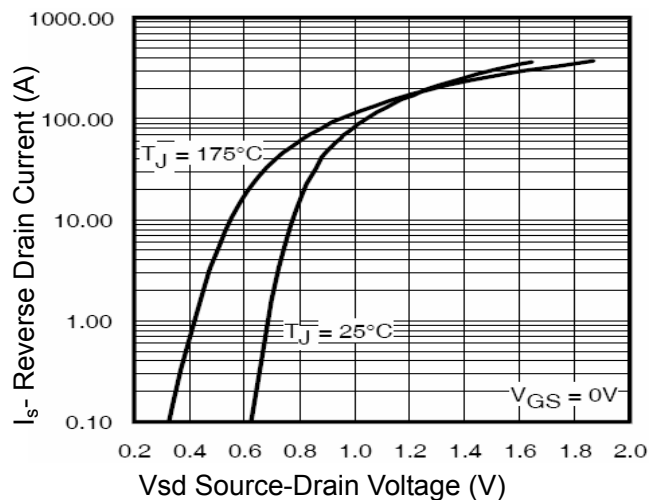
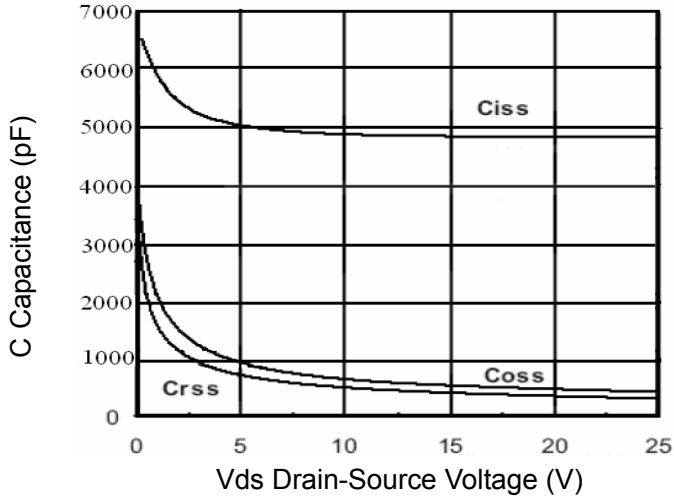
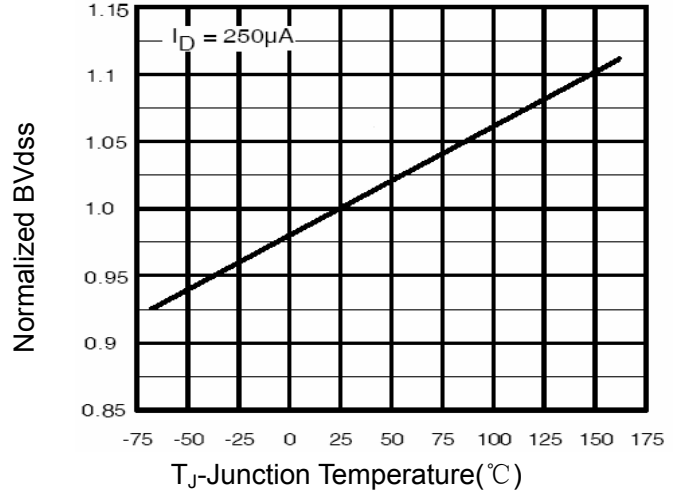


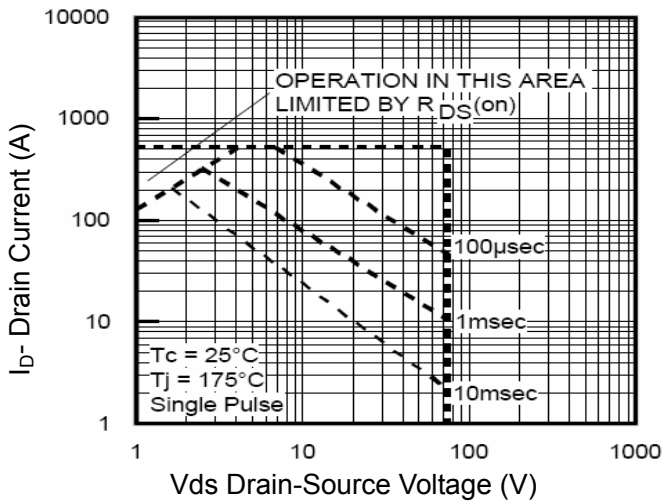
Figure 6 Source- Drain Diode Forward



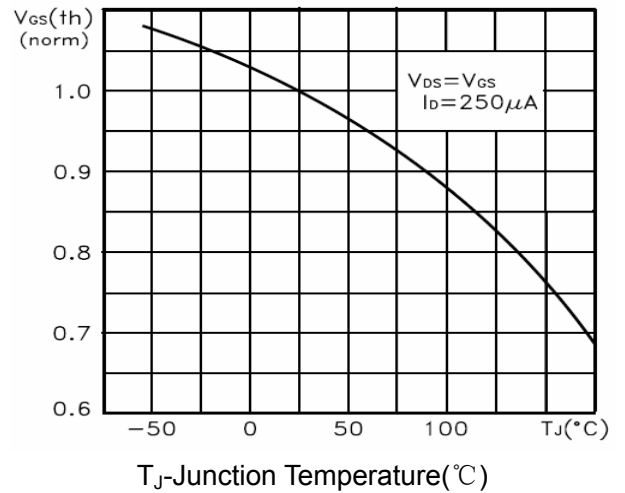
**Figure 7 Capacitance vs Vds**



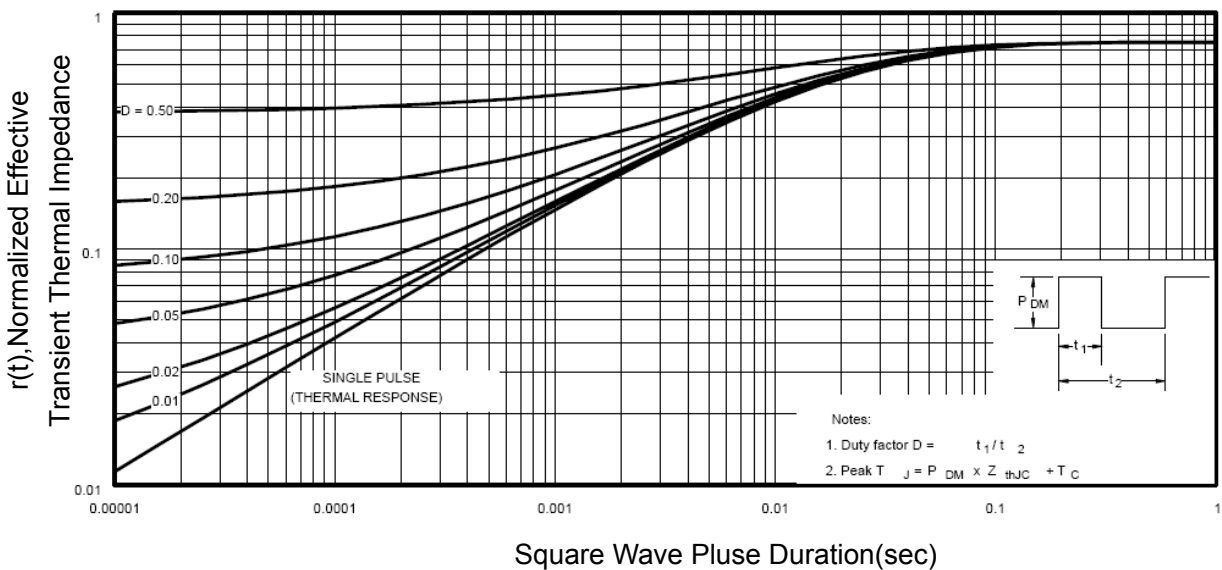
**Figure 9  $BV_{DSS}$  vs Junction Temperature**



**Figure 8 Safe Operation Area**



**Figure 10  $V_{GS(th)}$  vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

# Package Information

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